REMARKS/ARGUMENTS

Claims 1 through 22 were pending in this application. The present Amendment amends claims 1 and 18 and adds new dependent claims 23 and 24. Reconsideration and favorable action are respectfully requested.

Rejections Under 35 U.S.C. § 102

Claims 1-22 are rejected under 35 U.S.C. § 102(b) as being anticipated by Jaggar (US Patent 6,343,358, hereafter "Jaggar").

The Examiner cites to text in Jaggar but does not expressly indicate which element in Jaggar corresponds to which element in each rejected claim. For example with respect to claim 1, the Examiner does not identify what structure the Examiner finds in Jaggar as the recited "memory" of claim 1. Is the Examiner referring to Jaggar data transfer register DTR, which Jaggar details in Figure 3 as two separate registers? Or, is the Examiner referring to the "memory" cited in line 2 of Jaggar column 6, which Jaggar expressly states is "not shown" and for which virtually no detail is provided. In any event, to advance prosecution of the present application and without prejudice, limitation or disclaimer, independent claims 1 and 18 are amended and Applicant respectfully requests withdrawal of the present rejection, with additional details stated below.

Claim 1 previously recited that its memory structure comprises "an integer *M* of memory word slots," and claim 1 is now amended to recite that "the integer *M* is greater than one." Thus, to the extent that the Examiner might be contending that a transfer register of Jaggar is a memory structure per claim 1, Jaggar does not show such a register having more than one word slot. To the extent the Examiner might be contending that the two transfer registers (i.e., wDTR and rDTR) of Jaggar are a memory structure per claim 1, then Jaggar does not anticipate the remainder of the claim. For example, claim 1 separately recites control circuitry that operates with respect to "all of" the memory word slots, and those memory word slots are of "an integer number *M* greater than one" and "arranged in a first-in first-out configuration." Jaggar does not show these recitations.

Thus, the recitations of amended claim 1 are neither shown, suggested, nor taught by Jaggar, and, therefore, Applicant respectfully requests that the present rejection be withdrawn. From the above, Applicant respectfully submits that amended claim 1, and its dependent claims 2-17 and 23 are patentable over the cited rejections and thereby are in condition for allowance.

Independent claim 18 is rejected for the same reasons as set forth above with respect to claim 1, and it is amended in a manner comparable to claim 1. Thus, Applicant respectfully submits that amended claim 18, and its dependent claims 19-22 and 24 are patentable over the cited rejections and thereby are in condition for allowance.

Lastly, Applicant respectfully traverses various of the findings of the Examiner with respect to Jaggar. By ways of examples but not by exhausting all instances, as a first example the Examiner in section 3 of the Action states that Jaggar teaches writing to "***all of*** the memory words slots of the memory strucuture" and reading from "***all of*** the memory words slots of the memory strucuture" – Applicant respectfully submits that such a teaching is not stated by Jaggar. As a second example, the Examiner in section 8 of the Action states that Jaggar teaches comparing scan words to the test sequence – Applicant respectfully submits that such a teaching is not stated by Jaggar. As still another example, the Examiner in section 9 of the Action states that Jaggar teaches latches, but Jaggar appears to be completely silent as to the construction of the storage devices at the textual locations provided by the Examiner.

New claims

New claims 23 and 24 are added, depending respectively from independent claims 1 and 18. Each of these new claims recites a "***single*** serial shift storage circuit," which differs therefore from Jaggar which in its Figure 3 shows two different serial shift registers wDTR and rDTR that may each be said to have *N* bit but which therefore combine to provide 2*N* bits, in contrast to the recitations of claims 23 and 24. Thus, these claims are allowable over Jaggar.

Fees

A Petition for an Extension of Time for two (2) months is submitted herewith, thereby extending the deadline from July 21, 2008 to September 22, 2008 (as September 21, 2008 falls on a Sunday). The Commissioner is therefore authorized to charge the fee for this Petition, the fees for the two new dependent claims submitted herewith, and any other fees necessary to effect the present filing, to Deposit Account 20-0668 of Texas Instruments Incorporated.

Conclusion

Applicant respectfully requests that a timely Notice of Allowability be issued in this case.

Respectfully submitted,

/stephen l. levine/

Stephen L. Levine
Registry No. 33,413

Anderson, Levine & Lintel, L.L.P.
14785 Preston Road, Suite 650
Dallas, Texas 75254
(972) 664-9552
September 22, 2008

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37 C.F.R. 1.8

The undersigned hereby certifies that this correspondence is being transmitted via PAIR e-filing, **on September 22, 2008,** to the United States Patent Office.

/stephen l. Levine/

Stephen L. Levine
Registry No. 33,413